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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,237	12/15/2003	John Chiang	64965-172	2279

7590 02/27/2007

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EXAMINER	
PHAN, MAN U	
ART UNIT	**PAPER NUMBER**
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,237	CHIANG, JOHN	
	Examiner	Art Unit	
	Man Phan	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Chiang for the "Method and apparatus for locking a table in a network switch" filed 12/15/2003 has been examined. This application is a Continuation of the application 09/296,558 filed 04/22/1999. The preliminary amendment filed 12/15/2003 has been entered and made of record. Claims 1-16 are pending in the application.

2. The applicant should use this period for response to thoroughly and very closely proof read and review the whole of the application for correct correlation between reference numerals in the textual portion of the Specification and Drawings along with any minor spelling errors, general typographical errors, accuracy, assurance of proper use for Trademarks ™, and other legal symbols @, where required, and clarity of meaning in the Specification, Drawings, and specifically the claims (i.e., provide proper antecedent basis for "the" and "said" within each claim). Minor typographical errors could render a Patent unenforceable and so the applicant is strongly encouraged to aid in this endeavor.

Drawings

3. The informal drawings are not of sufficient quality to permit examination. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a). Failure to timely submit replacement drawing sheets will result in ABANDONMENT of the application.

Claim Objections

4. Claim 7 is objected to because of the following informalities:

This claim combines claim 8 at the end (lines 6-10) by typographic error. Appropriate correction is required.

Claim Rejections - 35 USC ' 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 recites limitation "the multiport switch" in line 4.

Claim 5 recites limitation "the plural entries" in line 2.

There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled

the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

7. Claims 10 and 11 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Runaldue et al. (US#6,052,751).

Regarding claim 10, Runaldue et al. disclose a scalable multiport switch that receives and transmits data through a plurality of ports is provided with a plurality of internal buses, an external memory interface, and a slot manager (scheduler). Runaldue teaches an arrangement for controlling access to information stored within a network switch depicted in Fig. 16A comprising: an address table for storing entries that contain addresses of network stations connected to the network switch and a plurality of components capable of accessing the address table (Col. 23, lines 25-31) a scheduler for allocating prescribed time slots to the plurality of components for accessing the address table (Col. 14, lines 9-16 and Col. 24, lines 51-57). Runaldue et al. further teaches wherein each of the components being configured for determining if any other components are currently transacting with the address table during its allocated time slot (Col. 8, lines 6-12, and Col. 22, lines 63-67), and accessing the address table if none of the other components are currently transacting with the address table (Col. 12, lines 24-30, and Col. 14, lines 2-16)

Regarding claim 11, Runaldue et al. further discloses a buffer manager of the switch subsystem and port vector FIFO depicted in Fig. 14 in which when the address table is being accessed, a designated component of the plurality of components is configured to wait until the scheduler allocates another time slot to the designated component in order to determine if any other components are currently transacting with the address table (See Fig. 14; Col. 23, lines 5-8, and lines 18-20)

Runaldue et al. (US#6,052,751) is applied herein merely for the teaching of a method and arrangement for controlling access information stored within a network switch comprising an address table for storing entries that contain addresses of network stations connected to the network switch and a plurality of components capable of accessing the address table (Col. 23, lines 25-31); a Slot manager (scheduler) for allocating prescribed time slots to the plurality of components for accessing the address table (Col. 14, lines 9-16 and Col. 24, lines 51-57). It's noted that the "address table" is an example of an address table storage (i.e., memory) for storing address information relating to the ports (addressable memory). Runaldue discloses a multiport switch that receives and transmits data through a plurality of ports, storing data in a memory and controlling access to a memory. A memory interface is often employed to control the access from the sources to the memory. Fig. 14 illustrated a block diagram of a queuing block of the buffer manager of the switch subsystem and a port vector FIFO, in which the port vector FIFO 70 queries the address table 160 with the frame pointer.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 12 -16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Runaldue et al. (US#6,052,751) as applied to claims 10-11 above, in view of Fried et al. (US#5,142,676).

With respect to claims 12, 13, the references disclose a novel system and method for dynamically allocating bandwidth to applications in a network based on utility functions, according to the essential features of the claims. Runaldue et al. disclose the claimed limitations discussed in paragraph 8 above. However, Runaldue et al. do not disclose that a designated component of the plurality of components is configured to assert a lock signal indicating that the designated component is currently transacting with the address table. In the same field of endeavor, Fried et al. (US#5,142,676) discloses a multiprocessor system incorporating the locking circuit depicted in Fig. 3 comprising a LOCK signal supplied to gate 104 is asserted, and the DISALLOW signal is asserted, thereby inhibiting completion of the memory access cycle. Otherwise, completion of the memory access cycle is enabled (Col. 3, lines 3 to Col. 4, lines 20). Regarding claim 14, Fried et al. further teaches a locking circuit for controlling access to locked segments of a shared memory. The locking circuit comprises a content addressable memory for storing addresses of the locked memory segments and for comparing a target address with the addresses of the locked memory segments and providing a match signal when the target address matches one of the addresses of the locked memory segments (Col. 2, lines 28-37).

Regarding claim 15, Fried et al. teaches in Fig. 1 depicted a simplified block diagram of a multiprocessor system incorporating the locking circuit locking circuit for controlling access to a shared memory wherein lock checking is performed comprising a CPU connectable to the network switch, a processor interface for interfacing the CPU to network switch and being configured to receive request to access the address table from the CPU (Col. 3, lines 31-39);

determine if any components of the network switch are currently transacting with the address table and indicate to the CPU that the address table is available for use if no other components of the network switch are currently transacting with the address table (Col. 3, lines 40-63). Regarding claim 16, Fried further teaches in Fig. 3 depicted the control section of the locking circuit in accordance with the present invention in which the processor interface is configured to set an acknowledge bit to indicate that the address table is not being used, and the CPU is configured to access the address table upon detecting that the acknowledge bit is set (See Fig. 2; Col. 5, lines 34-59).

One skilled in the art would have recognized the need for effectively and efficiently controlling access to an address table in a network switch, and would have applied Fried's novel use of locking circuit for controlling access to shared memory using asserted signals into Runaldue's teaching of a multiport switch that receives and transmits data through a plurality of ports using the slot manager for scheduling access to the address table. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Fried's separate content addressable memories for storing locked segment addresses and locking processor identifications for controlling access to shared memory's into Runaldue's method and apparatus for changing the number of access slots into a memory with the motivation being to provide a system and method for controlling access to an address table in a network switch.

10. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Runaldue et al. (US#6,052,751) as applied to claims 10-11 above, in view of Fried et al. (US#5,142,676).

Regarding claim 1, both of these references teaches the capability of effectively and efficiently controlling access and locking mechanism in a shared resource system. Runaldue et al. disclose the claimed limitations discussed in paragraph 7 above. However, Runaldue et al. do not disclose the step of locking out the designated component from accessing the address table, if one of the other components is currently transacting with the address table. In the same field of endeavor, Fried et al. discloses a multiprocessor system incorporating the locking circuit depicted in Fig. 3 comprising a LOCK signal supplied to gate 104 is asserted, and the DISALLOW signal is asserted, thereby inhibiting completion of the memory access cycle. Otherwise, completion of the memory access cycle is enabled (Col. 3, lines 3 to Col. 4, lines 20).

Regarding claim 2, Runaldue et al. further discloses a buffer manager of the switch subsystem and port vector FIFO depicted in Fig. 14 in which when the address table is being accessed, a designated component of the plurality of components is configured to wait until the scheduler allocates another time slot to the designated component in order to determine if any other components are currently transacting with the address table (See Fig. 14; Col. 23, lines 5-8, and lines 18-20).

Regarding claim 6, Fried et al. further teaches a locking circuit for controlling access to locked segments of a shared memory. The locking circuit comprises a content addressable memory for storing addresses of the locked memory segments and for comparing a target address with the addresses of the locked memory segments and providing a match signal when the target address matches one of the addresses of the locked memory segments (Col. 2, lines 28-37).

Associated with each locked memory address in table 24 is a locking processor identification (ID) which identifies the processor that caused that memory segment to be locked. As described, the locking processor ID is used to permit access to the locked memory segment by the locking processor, while blocking access by other processors (Col. 3, lines 57-63).

Claims 3-5 and 7-9 are method claims corresponding to apparatus claims 12-14 and 15-16 respectively. Therefore, the steps read on the corresponding limitations as set forth, and they are analyzed, rejected as previously discussed.

One skilled in the art would have recognized the need for effectively and efficiently controlling access to an address table in a network switch, and would have applied Fried's novel use of locking circuit for controlling access to shared memory using asserted signals into Runaldue's teaching of a multiport switch that receives and transmits data through a plurality of ports using the slot manager for scheduling access to the address table. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Fried's separate content addressable memories for storing locked segment addresses and locking processor identifications for controlling access to shared memory's into Runaldue's method and apparatus for changing the number of access slots into a memory with the motivation being to provide a system and method for controlling access to an address table in a network switch.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Merchant et al. (US#6,480,490) is cited to show the interleaved access to address table in network switching system.

The Kerstein (US#6,292,483) is cited to show the apparatus and method for generating an index key for a network switch routing table using a programmable hash function.

The Chao (US#5,915,097) is cited to show the method and apparatus for data storage and search in an address table of an ethernet switch.

The Riley et al. (US#5,856,972) is cited to show the duplicate message detection method and apparatus.

The Erimli (US#6,483,844) is cited to show the method and apparatus for sharing an external memory between multiple network switches.

The Miller et al. (US#6,112,258) is cited to show the multiple-cycle I/O ASIC communication system having an arbiter circuit capable of updating address table associated with each I/O ASIC on bus.

The Lau et al. (US#6,463,032) is cited to show the network switching system having overflow bypass in internal rules checker.

The Egbert et al. (US#6,115,387) is cited to show the method and apparatus for controlling initiation of transmission of data as a function of received data.

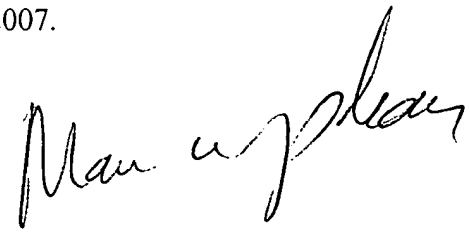
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached on Mon - Fri from 6:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin, can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at toll free 1-866-217-9197.

Mphan

02/21/2007.



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